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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/572,655 | 03/06/2007 | Dominik Eisert | 5367-223PUS | 4408 |

7590 06/29/2010
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| EXAMINER |
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LAM, CATHY N

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| ART UNIT | PAPER NUMBER |
|----------|--------------|

2811

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| MAIL DATE | DELIVERY MODE |
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06/29/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| | | | |
|------------------------------|--------------------------------------|--------------------------------------|--|
| Office Action Summary | Application No. 10/572,655 | Applicant(s) EISERT ET AL. | |
| | Examiner CATHY N. LAM | Art Unit 2811 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04/14/2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-8,10-18 and 44-73 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-8,10-18 and 44-73 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>01/25/2010, 06/07/2010</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-2, 4-8, 10-18, 44-73, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lester (U.S. Patent No. 6,291,839).

Regarding claim 1, Lester discloses in figure 5 a radiation (light) emitting semiconductor chip comprising:

an epitaxial multilayer structure 16, 14, 8, fig. 5 comprising:

an active radiation (light) generating layer 14

a first main face (bottom surface of layer 8) and

a second main face (upper surface of layer 16) remote from the first main face for coupling out radiation generating in the active radiation generating layer 14, and

a reflective layer 9 or interface, and

wherein the first main face of the multilayer structure is coupled to the reflective layer 9 or interface, and

wherein a patterned region 16 of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by either one or two dimensional fig.1 depressions forming convex elevations (truncated pyramids) fig.5.

It is noted that the term "thin film" is a broad limitation herein because there is no recitation of how thin this thin film is in specific. Therefore, the film disclosed by Lester in figure 5 can be construed as "thin film".

Lester discloses the claimed invention except for the convex elevations having a height (h1) at least as large as a distance (h2) between the patterned region and the active, radiation-generating layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the convex elevations of a height (or depth) as taught by Lester (col.5, lines 8-18) to have a height (h1) at least as large as a distance (h2) between the patterned region and the active, radiation-generating layer as of the claimed invention, in order to scatter light in the semiconductor layer and increase the extraction efficiency (col.5, lines 8-18). Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In *re Aller*, 105 USPQ 233.

Regarding claim 46, Lester discloses a radiation-emitting thin-film semiconductor chip comprising an epitaxial multilayer structure and a reflective layer or interface, the epitaxial multilayer structure comprising:

an active, radiation-generating layer 14,

a first main face (bottom surface of layer 8), and

a second main face (upper surface of layer 16) remote from the first main face for coupling out the radiation generated in the active, radiation-generating layer 14,

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wherein the first main face of the multilayer structure is coupled to the reflective layer 9 or interface, and

wherein a patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by either one- or two dimensional (figs.1,5) depressions forming convex elevations (truncated pyramids).

It is noted that the term "thin film" is a broad limitation herein because there is no recitation of how thin this thin film is in specific. Therefore, the film disclosed by Lester in figure 5 can be construed as "thin film".

Lester discloses the claimed invention except for the convex elevations having an inclination angle (B) of between approximately 30° and approximately 70°.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the convex elevations having an inclination angle as taught by Lester to the convex elevations having an inclination angle (B) of between approximately 30° and approximately 70° as of the claimed invention, in order to scatter light in the semiconductor layer and increase the extraction efficiency (col.5, lines 8-18). Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In *re Aller*, 105 USPQ 233.

Regarding claims 2, 48, Lester discloses the semiconductor chip as claimed in claim 1, further comprising a carrier element coupled to the first main face, wherein the

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reflective layer 9 or interface is arranged between the carrier element and the multilayer structure.

It is noted that the substrate as shown in figure 5 can function as "carrier substrate" because it is connected to reflector 9, which enables the substrate to electrically connect with the electrical source or circuit to drive the light emitting device

Regarding claims 4, 5, 49, 50, Lester discloses in figure 5 the semiconductor chip as claim 1, wherein the elevations of layer 16 have a form of truncated pyramids or truncated cones or a trapezoidal cross sectional form or a form of cones or a triangular cross-section form fig.5.

Regarding claim 6, Lester discloses in figure 5 the elevations 16 have a form of truncated cones, not of a circle or sphere segment cross sectional form as claimed.

However In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966), the Court held that the changes in shape was a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence (MPEP 2144.04, page 2100-137, Rev. 5, August, 2006).

It would have been obvious to one having ordinary skill in the art at the time of the present invention was made to modify Lester by including the elevation having the circle segment cross sectional form, since this involves only routine skill in the art.

Regarding claims 7, 8, 51, Lester discloses in figure 5 the elevations have an aperture angle of certain degree(s), not necessarily between approximately 30° and approximately 70° or between approximately 40° and approximately 50°.

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It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Lester by including the elevations having an aperture angle of between approximately 30° and approximately 70° or between approximately 40° and approximately 50° , since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 10, 52, 53, Lester discloses in figure 5 the elevations 16 have certain heights.

Lester does not disclose the height (h_1) of the elevations being approximately as large as or twice as large as the distance (h_2) between the patterned region of the multilayer structure and the active, radiation generating layer.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made, to modify Lester by including the height of the elevations being approximately twice as large as the distance between the non patterned region of the multilayer structure and the active, radiation generating layer and the elevation, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 11, 54, Lester discloses in figure 5 the elevations have a light emitted opening dimension.

Lester does not disclose the cell size (d) of the elevations being at most approximately five times as large as the height (h_1) of the elevations.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify Lester by including a light emitted opening dimension of the elevations being at most approximately five times as large as the height of the elevations, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272,205 USPQ 215 (CCPA 1980).

Regarding claims 12, 55, Lester discloses in figure 5 the elevations have a light emitted opening dimension.

Lester does not disclose the cell size of the elevations being at most approximately three times as large as the height of the elevations.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made, to modify Lester by including the light emitted opening dimension of the elevations being at most approximately three times as large as the height of the elevations, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 13, as best understood, Lester discloses in figure 5 the reflective layer 9 or interface coupled to the first main area of the multilayer structure has a reflection at least 70% (column 2, lines 65-66).

Regarding claims 14, 56, Lester discloses in column 2, lines 65-67 the layer 9 coupled to the first main area of the multilayer structure has a reflection of at least 70%.

Lester does not exclusively discloses a reflectivity of at least 85%.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify Lester by including the layer or interface couple to the first main area of the multilayer structure as a reflectivity of at least 85%, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 15, Lester discloses in figure 5 the multilayer structure is applied on a carrier substrate (substrate) either directly by its first main face or via a reflective layer.

It is noted that the substrate as shown in figure 5 can function as "carrier substrate" because it is connected to reflector 9, which enables the substrate to electrically connect with the electrical source or circuit to drive the light emitting device.

Regarding claim 16, Lester discloses in figure 5 the reflective layer 9 is also a conductive layer (col.3 lines 49-50) which can serve as a contact layer of the semiconductor component.

Regarding claim 17, Lester discloses in figure 5 a conductive transparent layer 20 (column 3, lines 41-48) applied onto the second main face of the multilayer structure.²

Regarding claims 18, 60, Lester discloses a conductive transparent chip as claimed in claim 1, further comprising a transparent protective layer 22 (col.4 lines 62-66) applied onto the second main face of the multilayer structure.

Regarding claim 44, Lester discloses the semiconductor chip as claimed in claim 1, wherein each of the convex elevations is defined by two-dimensional depressions fig.1.

Regarding claims 45, 47, Lester discloses the semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer of the semiconductor chip is free of a growth substrate.

Regarding claim 57, Lester discloses the semiconductor chip as claimed in claim 47, wherein the multilayer structure is applied onto a carrier substrate either directly by the first main face or via the reflective layer or interface fig.5.

Regarding claim 58, Lester discloses the semiconductor chip as claimed in claim 57, wherein the reflective layer 9 or interface or the carrier substrate serves as a contact layer of the semiconductor chip, as well known in the art, in order for the semiconductor chip enables to contact with the electrical source or circuit to drive the light emitting device.

Regarding claim 59, Lester discloses the semiconductor chip as claimed in claim 46, further comprising a conductive, transparent layer 22 (col.4 lines 62-66) applied onto the second main face of the multilayer structure fig.4.

Regarding claim 61, Lester discloses the semiconductor chip as claimed in claim 46, wherein the multilayer structure comprises a material or a plurality of different materials based on GaN (abstract).

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Regarding claim 62, Lester discloses the semiconductor chip as claimed in claim 1, wherein the second main face is a noncontinuous layer (the surface has many recess) fig.5.

Regarding claim 63, Lester discloses the semiconductor chip as claimed in claim 1, wherein the reflective layer 9 is in direct contact with the epitaxial multilayer structure fig.5.

Regarding claim 64, Lester discloses the semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on a II-VI semiconductor material (GaN, col.5 line27).

Regarding claim 65, Lester discloses the semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on a phosphide compound semiconductor material (col.5 line 20).

Regarding claim 66, Lester discloses the semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on an arsenide compound semiconductor material (col.5 line 20).

Regarding claim 67, Lester discloses the semiconductor chip as claimed in claim 1, wherein the patterned region of the multilayer structure that adjoins the second main face (top surface of layer 16) of the multilayer structure is patterned by two-dimensional fig.1 depressions forming convex elevations fig.5.

Regarding claim 68, Lester discloses the semiconductor chip as claimed in claim 46, wherein the second main face is a noncontinuous layer (a noncontinuous with recesses) fig.5.

Regarding claim 69, Lester discloses the semiconductor chip as claimed in claim 46, wherein the reflective layer 9 is in direct contact with the epitaxial multilayer structure fig.5.

Regarding claim 70, Lester discloses the semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on a II-VI semiconductor material (GaN, col.5 line27).

Regarding claim 71, Lester discloses the semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on a phosphide compound semiconductor material (col.5 line 20).

Regarding claim 72, Lester discloses the semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on an arsenide compound semiconductor material (col.5 line 20).

Regarding claim 73, Lester discloses the semiconductor chip as claimed in claim 46, wherein the patterned region of the multilayer structure that adjoins the second main face (top surface of layer 16) of the multilayer structure is patterned by two-dimensional fig.1 depressions forming convex elevations fig.5.

Response to Arguments

3. Applicant's arguments filed 04/14/2010 have been fully considered but they are not persuasive.

4. In response to Applicant's remarks regarding claims 1 and 46 filed 04/14/2010, pages 10-14, the Examiner recognizes the Applicant's position; however, the claim does not preclude the Examiner's interpretation of the new limitation. Applicant remarks regarding that "Lester's structure contains concave etched holes formed in the p-type layer 16 (see, also, Fig. 5 of Lester), rather than convex elevations formed by one- and two-dimensional depressions expressly recited in independent claims 1 and 46". As in the updated rejection of claims 1 and 46 above, the Examiner recognizes that fig.5 of Lester discloses the claimed invention of claims 1 and 46. The claimed of claims 1 and 46 are not clearly specify the terms "convex elevation" which made it different with the prior art of record from a top view. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Accordingly, the cross sectional view of Lester of fig.5 is not different with the cross sectional view of the claimed invention of fig.1, therefore, fig.5 of Lester reads the claimed limitations of claims 1 and 46.

5. In response to Applicant's remarks regarding that "Lester's layer 20 with etched holes is a current-spreading layer used to spread the current for driving Lester's device over the entire p-side (see, e.g., col. 3, 11. 11-15 or col. 2, 11. 18-23 of Lester).

Consequently, one skilled in the art would not modify the etched holes of Lester to one-

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or two-dimensional depressions forming convex elevations as such elevations would not allow for a continuous layer 20 necessary for spreading current impressed by p-contact pad 21 over the entire p-side (see Fig. 1 of Lester)", the Examiner recognizes the argument is taken to be mere statements of intended use which does not add any structure, therefore it has not been given any patentable weight. Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." (emphasis in original) Hewlett - Packard Co. V. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). In apparatus, article, and composition claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CATHY N. LAM whose telephone number is (571)270-5021. The examiner can normally be reached on M-F 7:30AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, LYNNE GURLEY can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CL
06/22/2010

/Cuong Q Nguyen/

Primary Examiner, Art Unit 2811

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